What is claimed is:

1. A programmable logic device, comprising:

a function cell that provides a result logic value in response to one or more input logic values and a function vector, the function cell having an arithmetic logic circuit that in a first mode is operable to provide the result logic value as an arithmetic combination of the input logic values and in a second mode is operable to provide the result logic value as a logical combination of the input logic values, the arithmetic combination and the logical combination both determined by the function vector.

2. A programmable logic device according to claim 1, wherein the first and second modes are defined by a received arithmetic mode enable signal, the arithmetic logic circuit being operable to determine the defined mode from the received arithmetic mode enable signal.

3. A programmable logic device according to claim 1, wherein the arithmetic logic circuit further provides a carry output in response to the input logic values, the function vector and a carry input.

4. A programmable logic device according to claim 1, wherein the arithmetic combination is one of an add, a subtract, an increment, and a decrement operation.

5. A programmable logic device according to claim 3, wherein the arithmetic combination is one of an add, a subtract, an increment, and a decrement operation.

6. A programmable logic device according to claim 1, wherein the logical combination is one of a NOR, an XOR, a NAND, an AND, an XNOR and an OR operation.

7. A programmable logic device according to claim 1, wherein the function cell is operable to receive the function vector from a configuration memory.

8. A programmable logic device according to claim 1, wherein the function cell is operable to receive the function vector from dynamic configuration signals.

9. A programmable logic device, comprising:

a function cell that provides a result logic value in response to one or more input logic values and a function vector, the function cell being operable to receive the function vector both from a configuration memory and from dynamic configuration signals.

10. A programmable logic device according to claim 9, wherein the function cell includes a function selection block that is operable to selectively receive the function vector in response to a received function overlay enable signal.

11. A programmable logic device according to claim 10, wherein the function selection block is further operable to selectively receive the function vector from among a plurality of stored function vectors based on a received dynamic selection signal.

12. A programmable logic device according to claim 10, further comprising a controller block coupled to the function cell that is operable to receive the dynamic configuration signals from a global interconnect and to provide the dynamic configuration signals and the function overlay signal to the function cell.

13. A programmable logic device according to claim 10, wherein the function cell further includes an arithmetic logic circuit that receives the function vector from the function selection block, the arithmetic logic circuit being operable in a first mode to provide the result logic value as an arithmetic combination of the input logic values and operable in a second mode to provide the result logic value as a logical combination of the input logic values, the arithmetic combination and the logical combination both determined by the function vector.

14. A programmable logic device, comprising:

a plurality of function cells that provide result logic values in response to one or more input logic values and a function vector, the function cells being operable to receive respective stored function vectors from a configuration memory and a dynamic function vector; and

a controller block coupled to the function cells that is operable to receive dynamic configuration signals and to commonly provide the dynamic function vector to the function cells.

15. A programmable logic device according to claim 14, wherein the function cells correspond to respective bit positions in a multi-bit operation, the dynamic function vector causing the plurality of function cells to perform respective bit-wise operations in the multi-bit operation.

16. A programmable logic device according to claim 15, wherein the function cells further provides a carry output in response to the input logic values, the function vector and a carry input.

17. A programmable logic device according to claim 15, wherein the multi-bit operation is one of an add, a subtract, an increment, and a decrement operation.

18. A programmable logic device according to claim 16, wherein the multi-bit operation is one of an add, a subtract, an increment, and a decrement operation.

19. A programmable logic device according to claim 15, wherein the multi-bit operation is one of a NOR, an XOR, a NAND, an AND, an XNOR and an OR operation.

20. A programmable logic device, comprising:

a plurality of function cells that each provide a respective result logic value in response to one or more input logic values and a function vector; and

a controller block coupled to the function cells that is operable to receive the respective result logic values and to logically combine them to produce an expanded logic value.

21. A programmable logic device according to claim 20, wherein the controller block further receives another expanded logic value from another plurality of function cells and is operable to combine the another expanded logic value with the respective result logic values to produce the expanded logic value.

22. A programmable logic device according to claim 20, wherein the function cells include a shift and join block, the shift and join block being operable to selectively cause an associated one of the function cells to output the respective result logic value of the associated function cell, or to output the respective result logic value of an adjacent function cell.

23. A programmable logic device, comprising:

a plurality of cluster blocks that communicate via a global interconnect, the cluster blocks including:

a controller block coupled to the global interconnect for receiving dynamic configuration signals and for providing an arithmetic mode signal in response;

a plurality of function cells that receive the arithmetic mode signal from the controller and provide a respective result logic value in response to one or more input logic values and a function vector, each function cell having an arithmetic logic circuit that in a first mode is operable to provide the result logic value as an arithmetic combination of the input logic values and in a second mode is operable to provide the result logic value as a logical combination of the input logic values, the arithmetic combination and the logical combination both determined by the function vector, the first and second mode being determined by the arithmetic mode signal.

24. A programmable logic device, comprising:

a plurality of cluster blocks that communicate via a global interconnect, the cluster blocks including:

a plurality of function cells that provide result logic values in response to one or more input logic values and a function vector, the function cells being operable to receive respective stored function vectors from a configuration memory and a dynamic function vector; and

a controller block coupled to the function cells that is operable to receive dynamic configuration signals and to commonly

provide the dynamic function vector to the function cells in response.